

# Loop Optimization in Presence of STT-MRAM Caches: a Study of Performance-Energy Tradeoffs

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## Code optimizations

```
for ( i = 0; i < N; i++ )
  for ( k = 0; k < M; k++ )
    for ( j = 0; j < N; j++ )
      C[i][j] += A[j][k] * B[i][k] + B[j][k] * A[i][k]
```

## Tiling

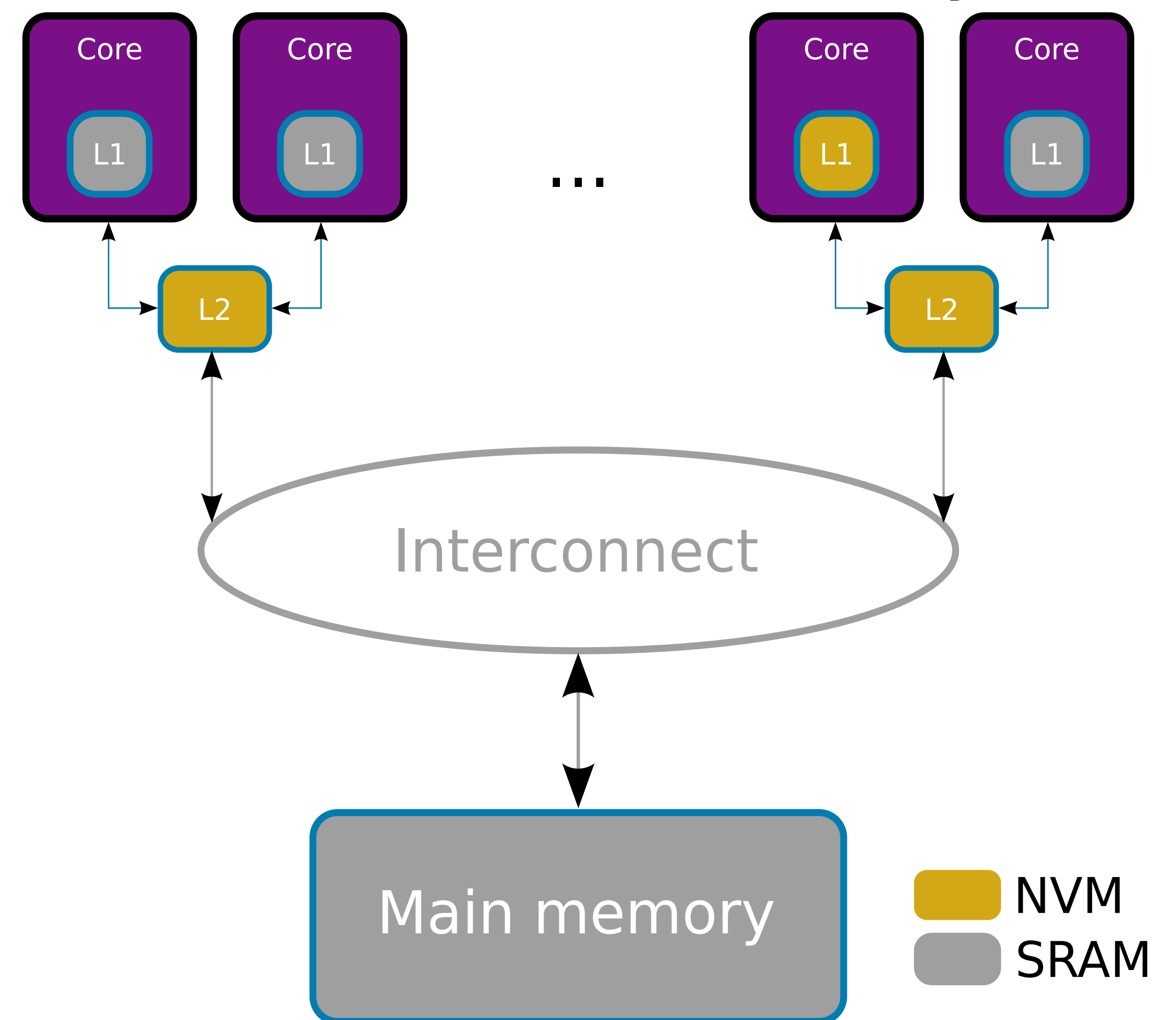
```
for ( ti = 0; ti < N; ti+=SI)
  for ( tk = 0; tk < M; tk+=SK)
    for ( tj = 0; tj < N; tj+=SJ)
      for ( i = ti; i < ti+SI; i++)
        for ( k = tk; k < tk+SK; k++)
          for ( j = tj; j < tj+SJ; j++)
            C[i][j] += A[j][k] * B[i][k] + B[j][k] * A[i][k]
```

or

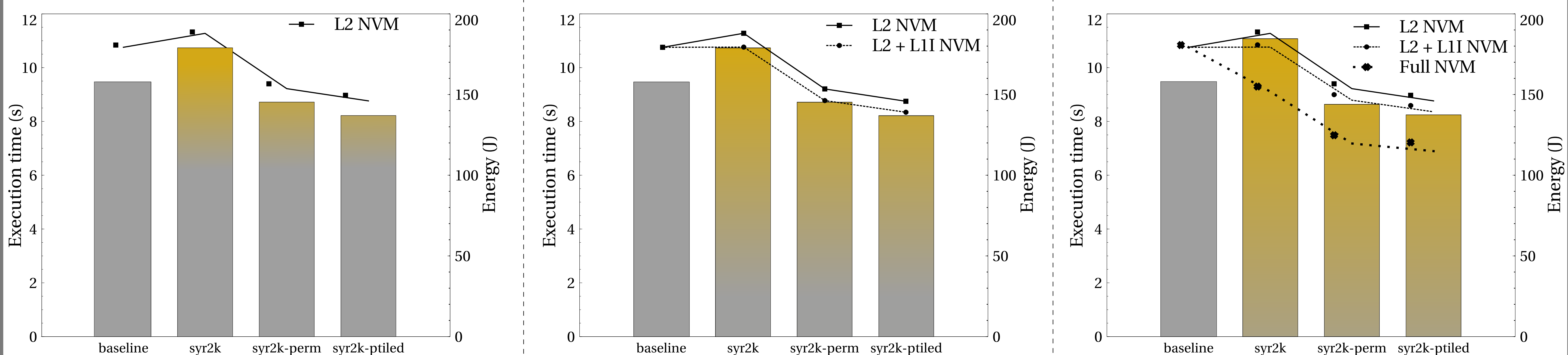
## Interchange

```
for ( i = 0; i < N; i++ )
  for ( j = 0; j < N; j++ )
    for ( k = 0; k < M; k++ )
      C[i][j] += A[j][k] * B[i][k] + B[j][k] * A[i][k]
```

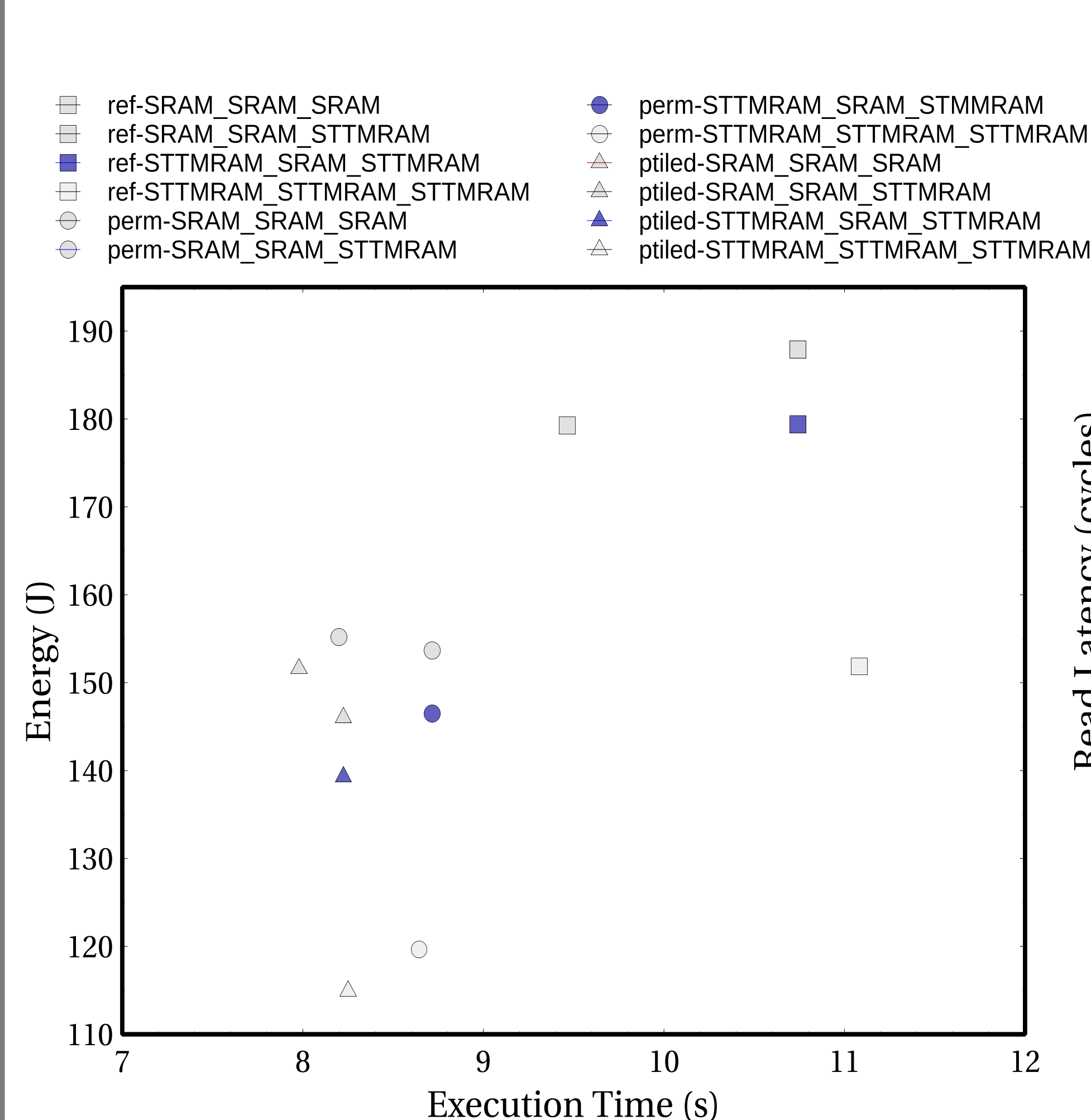
## Manycore architecture with Non Volatile Memory



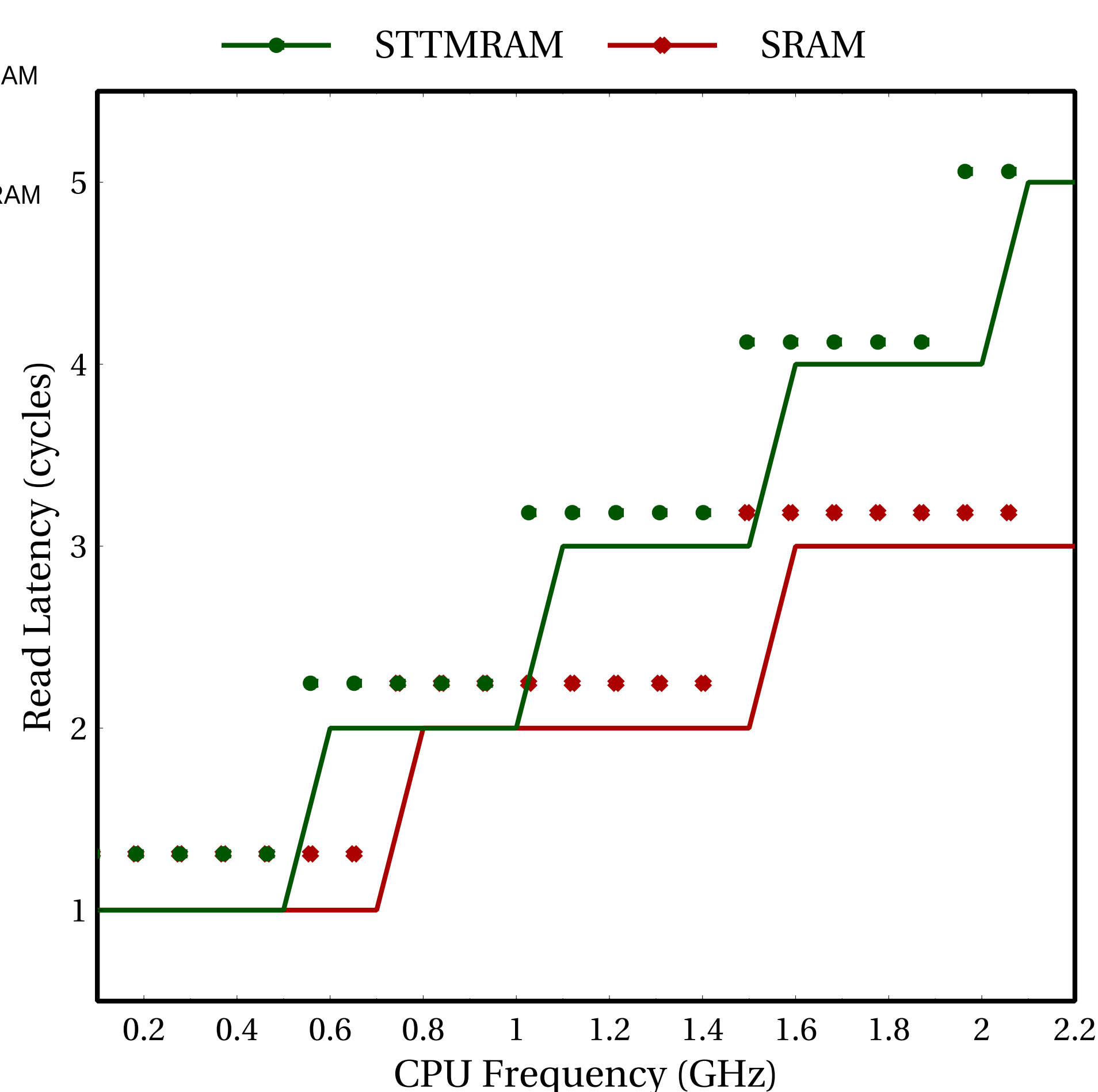
## Impact of NVMs on performance and energy



## Performance and energy tradeoff



## Operating frequency impact



## Gained insights

- Decreased power consumption (up to 31%)
- Negligible overhead (max 5.4%)
- Observed gain varies with memory operating frequency

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